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EXAMINER	
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ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,321	PACKER ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 26th of April 2004. Claims 1, 9-11, 15, 20, 21 and 27-29 have been amended; no claim has been canceled; and no claim has been newly added since Non-Final Office Action was mailed on 22nd of December 2003. Currently, claims 1-29 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over House et al. [US 5,274,783 A; hereinafter House] in view of Looi et al. [US 5,996,038 A; hereinafter Looi], Ehata [JP 2000181809 A] and IBM Technical Disclosure Bulletin ["Power Sequence Independent Expansion Bus Interface", TDB-ACC-NO: NN8606425, published by IBM, vol. 29, Issue No. 1, pages 425-426, on June 1, 1986; hereinafter IBM_TDB].

Referring to claim 1, House discloses a method for repeating communication signals by receiving said communication signals from one bus segment and outputting said communication signals to the other bus segment (See Abstract) in an I/O subsystem (i.e., computer system 10 in Fig. 1) having a plurality of bus segments (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1), each bus segment (e.g., segment of auxiliary SCSI bus in Fig. 1) having a set of devices (i.e., AUX-Bus peripheral devices 24 in Fig. 1) and a bus (i.e., Auxiliary Bus 28 of Fig. 1) that is coupled to said set of devices (See col. 4, lines 51-54), said I/O subsystem having at least one expander (e.g., Bus Extender 30 of Fig. 1), each expander being arranged to couple a pair of buses (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1) for propagating communication signals (See Fig. 1 and col. 4, line 63 through col. 5, line 2).

House does not expressly teach the steps of asserting a reset signal and resetting each expander and each device in response to said reset signal, i.e., a method steps for resetting bus segments to clear bus hang in said I/O subsystem.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein a method in said mechanism comprises a) asserting a reset signal (i.e., local bus reset signal) on a first bus segment (e.g., Expansion bus 61 in Fig. 1; See col. 4, lines 12-16); b) resetting each expander (i.e., bus expander bridge 60 of Fig. 1) coupled to said first bus segment (See col. 4, lines 4-6) and resetting each device (i.e., peripheral devices coupled to said bus 61 in Fig. 1) in said first bus segment (See col. 4, lines 16-20), i.e., a method steps for resetting bus segments (i.e., Buses 45, 64 and Expansion buses 51, 52, 61, 62 in Fig. 1) to clear bus hang in an I/O subsystem (i.e., computer system 10 of Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, in said method, as disclosed by House, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

House, as modified by Looi, does not teach each expander coupled to said first bus segment isolates said reset signal such that said reset signal is not propagated to the other bus segments.

Ehata discloses a SCSI control circuit (Fig. 2), wherein an expander (i.e., Reset-Condition Judging Circuit 7 of Fig. 2) coupled to a first bus segment (i.e., SCSI bus 3 of Fig. 2; e.g., as a hung-up SCSI device in Fig. 1) isolates a reset signal (i.e., RST signal of Fig. 2) such that said reset signal is not propagated to the other bus segments (e.g., not hung-up SCSI devices in Fig. 1; See col. 2 paragraph [0009] through col. 3, paragraph [0010]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said expander (i.e., Reset-Condition Judging Circuit), as disclosed by Ehata, in

said expander, as disclosed by House, as modified by Looi, so as to selectively reset only a bus segment (i.e., SCSI device) which has hung up by receiving said reset signal and resetting said hung-up bus segment when said hung-up bus segment is outputting a busy signal (See Ehata, col. 2, paragraphs [0005]-[0007]).

House, as modified by Looi and Ehata, does not expressly teach isolating all communication signals, and allowing propagation of communication signals between said first and other bus.

IBM_TDB discloses an expansion bus interface (See Figure), wherein c) for an expander (i.e., gate 3 in the Figure) coupled to a first bus segment (i.e., bus segment of local bus 13 in the Figure), c1) isolating all communication signals such that said expander (i.e., gate) prevents propagation of said communication signals between first bus (i.e., local bus 13 in the Figure) and other bus (i.e., external bus 18 in the Figure; See the second paragraph); c2) determining whether said other bus (i.e., external bus) is no longer hung (See the first paragraph, lines 9-10); c3) if said other bus is still hung, issuing a far-side reset signal (i.e., I/O RESET signal to I/O in the Figure) on said other bus to reset said other bus (See the first paragraph, lines 9-13); and c4) if said other bus is not hung, allowing propagation of communication signals between said first bus and said other bus (See the fourth paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said expander (i.e., gate 3 in the Figure), as disclosed by IBM_TDB, in expander, as disclosed by House, as modified by Looi and Ehata, so as to isolate said signals after isolating said reset signal for the advantage of prohibiting not hung-up bus segment (i.e., host system) inoperative from propagated faults in a hung-up bus segment (i.e., expansion unit) by said expander controller (i.e., circuit) which logically disconnects said hung-up bus segment (i.e., external bus in the external I/O unit) from said not hung-up bus segment (i.e., local bus in the host system) when a reset signal is asserted (i.e., when either a host system reset or an I/O unit power fault occurs; See IBM_TDB, the first paragraph).

Referring to claim 2, House, as modified by Looi, Ehata and IBM_TDB, discloses all the limitations of the claim 2 except that does not expressly teach if said other bus is still hung, operations b) and c) are repeated for other expanders coupled to each of said other buses.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have repeated said operations b) and c) for other expanders coupled to each of said other buses if said other bus is still hung, since it has been held that mere duplication of the essential working parts of said operations b) and c) for other expanders coupled to each of said other buses, involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

Referring to claim 3, Looi teaches each expander (e.g., bus expander bridge 60 of Fig. 1) enters into a reset isolation mode (i.e., reset state) in response to said reset signal (See col. 6, lines 26-31).

Referring to claim 4, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure) enters into a segment isolation mode (i.e., state of logically disconnected) to isolate all communication signals between said first bus and other bus (i.e., between local bus 13 and external bus 18 in the Figure; See the second paragraph).

Referring to claim 5, House teaches said I/O subsystem (i.e., computer system 10 in Fig. 1) is an SCSI I/O subsystem (See col. 4, lines 1-4) and wherein said other bus is no longer hung when said other bus is in a BUS FREE state (i.e., in fact that said computer system is using SCSI interface complying with SCSI standards implies that said other bus is no longer hung when said other bus is in a BUS FREE state).

Referring to claim 6, Looi teaches a host computer (i.e., processor 20 of Fig. 1) in said I/O subsystem (i.e., computer system 10 of Fig. 1) on said first bus segment (i.e., Expansion bus 61 in Fig. 1) asserts said reset signal on said first bus segment (See col. 4, lines 12-16 and 42-44).

Referring to claim 7, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure) exits said segment isolation mode (i.e., state of logically disconnected) when said other bus (i.e., external bus) is not

hung to allow said propagation of communication signals between said first bus and said other bus (See the fourth paragraph).

Referring to claim 8, Looi teaches said bus segments (i.e., Expansion bus 61 and Expansion bus 51 in Fig. 1) are reset one segment at a time from said first bus segment (i.e., Expansion bus 61 in Fig. 1; See col. 1, lines 6-10 and col. 6, lines 12-63).

4. Claims 9, 11, 12, 14, 15, 17, 19-21, 23, 24, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over House et al. [US 5,274,783 A; hereinafter House] in view of Ehata [JP 2000181809 A] and IBM Technical Disclosure Bulletin ["Power Sequence Independent Expansion Bus Interface", TDB-ACC-NO: NN8606425, published by IBM, vol. 29, Issue No. 1, pages 425-426, on June 1, 1986; hereinafter IBM_TDB].

Referring to claim 9, House discloses an expander device (i.e., Bus Extender 30 of Fig. 1) between a pair of bus segments (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1) in an I/O subsystem (i.e., computer system 10 in Fig. 1), each bus segment (e.g., segment of auxiliary SCSI bus in Fig. 1) having a set of devices (i.e., AUX-Bus peripheral devices 24 in Fig. 1) and a bus (i.e., Auxiliary Bus 28 of Fig. 1) that is coupled to said set of devices (See col. 4, lines 51-54), said expander device being arranged to couple said respective bus of a first bus segment (i.e., bus segment of main bus 26 in Fig. 1) of said pair to respective bus of a second bus segment (i.e., bus segment of auxiliary bus 28 in Fig. 1) of said pair for communication in said I/O subsystem (See col. 4, lines 55-62), said expander device including: a first I/O interface circuit (i.e., transceiver 42 of Fig. 3) configured to be coupled to said first bus segment (i.e., bus segment of main bus), said first I/O interface circuit being adapted to interface input and output communication signals with said first bus segment (See col. 5, lines 34-42); a second I/O interface circuit (i.e., transceiver 44 of Fig. 3) configured to be coupled to said second bus segment (i.e., bus segment of auxiliary bus) and being adapted to interface said input and output communication signals with said second bus segment (See col. 5, lines 34-42); and an expander controller (i.e., transfer circuits

46, 48 and control logic 50 of Fig. 3) arranged to communicate said input and output communication signals between said first and second I/O interface circuits, the expander controller being configured to control communication between said first and second bus segments (See col. 5, line 43 through col. 6, line 23).

House does not teach said expander controller includes a reset and segment isolation controller adapted to isolate a reset signal received on said first bus segment from propagating to said second bus segment, i.e., said expander device for isolating a reset between said pair of bus segments in said I/O subsystem.

Ehata discloses a SCSI control circuit (Fig. 2), wherein a reset and segment isolation controller (i.e., Inverter circuit 71 and OR circuit 72 in Fig. 2) adapted to isolate a reset signal (i.e., RST signal 6 of Fig. 2) received (See col. 2, paragraph [0004]) on a first bus segment (e.g., a hung-up SCSI device in Fig. 1) from propagating to a second bus segment (e.g., not hung-up SCSI device in Fig. 1), such that an expander device (i.e., SCSI control circuit in Fig. 2) for isolating a reset (i.e., RST signal) between said pair of bus segments in an I/O subsystem (i.e., SCSI bus system in Fig. 1; See col. 2 paragraph [0009] through col. 3, paragraph [0010]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reset and segment isolation controller (i.e., Inverter circuit and OR circuit), as disclosed by Ehata, in said expander controller, as disclosed by House, so as to selectively reset only a bus segment (i.e., SCSI device) which has hung up by receiving a reset signal and resetting said hung-up bus segment when said hung-up bus segment is outputting a busy signal (See Ehata, col. 2, paragraphs [0005]-[0007]).

House, as modified by Ehata, does not teach said expander controller isolates all signals to prevent propagation of said signals between said first and second bus segments after isolating a reset signal until said bus in said second bus segment is cleared from a hang condition.

IBM_TDB discloses an expansion bus interface (See Figure), wherein an expander controller (i.e., latch 2 and gate 3 in the Figure) isolates all signals to prevent propagation of said signals between a first bus segment (i.e., bus segment of local bus 13 in the Figure) and a second bus segment (i.e., bus segment of external bus 18 in the Figure) when a reset signal is asserted (See the second paragraph) until the bus (i.e., external bus 18 in the Figure) in said second bus segment is cleared from a hang condition (See the third and fourth paragraphs; i.e., wherein in fact that the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus implies that said expander controller isolates all signals until the bus in said second bus segment is cleared from a hang condition).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said expander controller (i.e., latch 2 and gate 3 in the Figure), as disclosed by IBM_TDB, in said reset and segment isolation controller, as disclosed by House, as modified by Ehata, so as to isolate said signals after isolating said reset signal for the advantage of prohibiting a non-fault bus segment (i.e., host system) inoperative from propagated faults in a fault bus segment (i.e., expansion unit) by said expander controller (i.e., circuit) which logically disconnects said fault bus segment (i.e., external bus in the external I/O unit) from said non-fault bus segment (i.e., local bus in the host system) when a reset signal is asserted (i.e., when either a host system reset or an I/O unit power fault occurs; See IBM_TDB, the first paragraph) after isolating said reset signal so as to selectively reset only said fault bus segment (i.e., SCSI device) by receiving said reset signal and resetting said fault bus segment (See Ehata, col. 2, paragraphs [0005]-[0007]).

Referring to claim 21, House discloses an SCSI expander (i.e., Bus Extender 30 of Fig. 1) between a pair of bus segments (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1) in an SCSI I/O subsystem (i.e., computer system 10 in Fig. 1), each bus segment (e.g., segment of auxiliary SCSI bus in Fig. 1) having a set of devices (i.e., AUX-Bus peripheral devices 24 in Fig. 1) and a bus (i.e., Auxiliary

Bus 28 of Fig. 1) that is coupled to said set of devices (See col. 4, lines 51-54), said SCSI expander being arranged to couple a first bus (e.g., main bus 26 in Fig. 1) in a first bus segment (i.e., bus segment of said main bus) and a second bus (i.e., auxiliary bus 28 in Fig. 1) in a second bus segment (i.e., bus segment of said auxiliary bus), said SCSI expander being configured to repeat communication signals by receiving said communication signals from one SCSI bus segment and outputting said communication signals to the other SCSI bus segment (See Abstract), said SCSI expander comprising: a first SCSI I/O interface circuit (i.e., transceiver 42 of Fig. 3) adapted to interface communication signals with said first SCSI bus segment (i.e., bus segment of main bus 26 in Fig. 1; See col. 5, lines 34-42); a second SCSI I/O interface circuit (i.e., transceiver 44 of Fig. 3) adapted to interface said communication signals with said second SCSI bus segment (i.e., bus segment of auxiliary bus 28 in Fig. 1; See col. 5, lines 34-42); and an SCSI expander controller (i.e., transfer circuits 46, 48 and control logic 50 of Fig. 3) coupled to communicate said communication signals between said first and second SCSI I/O interface circuits, said SCSI expander controller being arranged to control communication between said first and second SCSI bus segments (See col. 5, line 43 through col. 6, line 23).

House does not teach said SCSI expander controller includes a reset and segment isolation controller adapted to isolate a reset signal received on said first bus segment from propagating to said second bus segment, i.e., said SCSI expander device for resetting said bus segments to clear bus hang in said SCSI I/O subsystem.

Ehata discloses a SCSI control circuit (Fig. 2), wherein a reset and segment isolation controller (i.e., Reset-Condition Judging Circuit 7 of Fig. 2) adapted to isolate a reset signal (i.e., RST signal 6 of Fig. 2) received (See col. 2, paragraph [0004]) on a first bus segment (e.g., a hung-up SCSI device in Fig. 1) from propagating to a second bus segment (e.g., not hung-up SCSI device in Fig. 1), such that an SCSI expander device (i.e., SCSI control circuit in Fig. 2) for resetting said bus segments to clear bus hang in

said SCSI I/O subsystem (i.e., SCSI bus system in Fig. 1; See col. 2 paragraph [0009] through col. 3, paragraph [0010]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said reset and segment isolation controller (i.e., Reset-Condition Judging Circuit), as disclosed by Ehata, in said SCSI expander controller, as disclosed by House, so as to selectively reset only a bus segment (i.e., SCSI device) which has hung up by receiving a reset signal and resetting said hung-up bus segment when said hung-up bus segment is outputting a busy signal (See Ehata, col. 2, paragraphs [0005]-[0007]).

House, as modified by Ehata, does not teach said SCSI expander controller isolates all communication signals to prevent propagation of said communication signals between said first and second bus segments after isolating said reset signal until said second bus is in a BUS FREE state.

IBM_TDB discloses an expansion bus interface (See Figure), wherein an SCSI expander controller (i.e., latch 2 and gate 3 in the Figure) isolates all communication signals to prevent propagation of said communication signals between a first bus segment (i.e., bus segment of local bus 13 in the Figure) and a second bus segment (i.e., bus segment of external bus 18 in the Figure) when a reset signal is asserted (See the second paragraph) until said second bus is in a BUS FREE state (See the third and fourth paragraphs; i.e., wherein in fact that the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus implies that said expander controller isolates all communication signals until said second bus is in a BUS FREE state (viz., until the bus in said second bus segment is cleared from a hang condition)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said SCSI expander controller (i.e., latch 2 and gate 3 in the Figure), as disclosed by IBM_TDB, in said reset and segment isolation controller, as disclosed by House, as modified by Ehata, so as to isolate said signals after isolating said reset signal for the advantage of prohibiting a non-

fault bus segment (i.e., host system) inoperative from propagated faults in a fault bus segment (i.e., expansion unit) by said expander controller (i.e., circuit) which logically disconnects said fault bus segment (i.e., external bus in the external I/O unit) from said non-fault bus segment (i.e., local bus in the host system) when a reset signal is asserted (i.e., when either a host system reset or an I/O unit power fault occurs; See IBM_TDB, the first paragraph) after isolating said reset signal so as to selectively reset only said fault bus segment (i.e., SCSI device) by receiving said reset signal and resetting said fault bus segment (See Ehata, col. 2, paragraphs [0005]-[0007]).

Furthermore, the recitation that "an SCSI expander for resetting bus segments to clear bus hang in an SCSI I/O subsystem" which has been suggested by Ehata, has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *See Kropa v. Robie, 88 USPQ 478 (CCPA 1951).*

Referring to claim 11, IBM_TDB teaches if said bus in said second bus segment (i.e., External bus 18 in the Figure) is still hung, said expander controller (i.e., latch 2 and gate 3 in the Figure), which is said SCSI expander controller, issues a far-side reset signal (i.e., I/O RESET signal to I/O in the Figure) to said bus in said second bus segment to reset said second bus segment (See the fourth paragraph).

Referring to claim 23, IBM_TDB teaches if said second bus (i.e., External bus 18 in the Figure) is still hung, said expander controller (i.e., latch 2 and gate 3 in the Figure), which is said SCSI expander controller, issues a far-side reset signal (i.e., I/O RESET signal to I/O in the Figure) to said bus in said second bus segment to reset said second bus segment (See the fourth paragraph).

Referring to claims 12 and 24, IBM_TDB teaches said expander controller (i.e., latch 2 and gate 3 in the Figure) allows propagation of all signals between said first and second bus segments (i.e., local bus 13 and external bus 18 in the Figure) when said bus in said second bus segment (i.e., external bus) is

cleared from said hang condition (See the fourth paragraph), which means said second bus is in said BUS FREE state.

Referring to claims 14 and 26, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure), which is said SCSI expander controller, enters into a segment isolation mode (i.e., state of logically disconnected) to isolate all signals between said first and second bus segments (i.e., between local bus 13 and external bus 18 in the Figure; See the second paragraph).

Referring to claim 15, House teaches said I/O subsystem (i.e., computer system 10 in Fig. 1) is an SCSI I/O subsystem (See col. 4, lines 1-4) and wherein said bus in said second bus segment (i.e., auxiliary bus 28 of Fig. 1) is cleared from said hang condition when said bus in said second bus segment is in a BUS FREE state (i.e., in fact that said computer system is using SCSI interface complying with SCSI standards (See col. 2, lines 25-33) implies that said bus in said second bus segment (auxiliary SCSI bus) is cleared from said hang condition when said bus in said second bus segment is in a BUS FREE state).

Referring to claims 17 and 28, IBM_TDB teaches said each expander (i.e., gate 3 in the Figure), which is said SCSI expander controller, exits said segment isolation mode (i.e., state of logically disconnected) when said second bus segment (i.e., external bus) is not hung, which means said second bus is in the BUS FREE state, to allow said propagation of communication signals between said buses in said first and second bus segments (See the fourth paragraph).

Referring to claim 19, House, as modified by Ehata and IBM_TDB, suggests said reset and segment isolation controller (i.e., Inverter circuit 71 and OR circuit 72 in Fig. 2; Ehata) generates a reset isolation signal (i.e., output from OR circuit 71 of Fig. 2; Ehata), which is provided to reset output buffers (i.e., AND circuit 73 of Fig. 2; Ehata) in said first and second I/O interface circuits (i.e., transceivers 42 and 44 in Fig. 3; House) to disable propagation of said reset signal (i.e., RST signal 6 of Fig. 2; Ehata) to

said first and second bus segments (i.e., bus segments of main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1; House).

Referring to claim 20, House, as modified by Ehata and IBM_TDB, suggests said reset and segment isolation controller (i.e., LATCH 2 in the Figure; IBM_TDB) generates a segment isolation signal (i.e., I/O reset signal from latch 2 in the Figure; IBM_TDFB), which is provided to all output buffers in said first and second I/O interface circuits (i.e., GATE 3 of the Figure; IBM_TDB) to disable output of said communication signals (See IBM_TDB, the third and fourth paragraphs) from said first and second I/O interface circuits (i.e., transceivers 42 and 44 in Fig. 3; House) to said respective first and second bus segments (i.e., bus segments of main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1; House).

5. Claims 10, 13, 16, 18, 22, 25, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over House [US 5,274,783 A] in view of Ehata [JP 2000181809 A] and IBM_TDB ["Power Sequence Independent Expansion Bus Interface", TDB-ACC-NO: NN8606425, published by IBM, vol. 29, Issue No. 1, pages 425-426, on June 1, 1986] as applied to claims 9, 11, 12, 14, 15, 17, 19-21, 23, 24, 26 and 28 above, and further in view of Looi [US 5,996,038 A].

Referring to claims 10 and 22, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 10 and 22, respectively, except that does not teach said expander controller, which is said SCSI expander controller, is adapted to reset said expander device in response to said reset signal and wherein all devices in said first bus segment reset in response to said reset signal such that said bus in said first bus segment is cleared from said hang condition, which means said first bus is in said BUS FREE state.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein an expander controller (e.g., bus expander bridge 50 of Fig. 1) is adapted to reset an expander device (e.g., bus expander bridge 0 60 of Fig. 1) in response to a reset signal (See col. 6, lines 26-31) and wherein all

devices (e.g., peripheral devices coupled to said bus 61 in Fig. 1) in a first bus segment (i.e., Expansion bus 61 in Fig. 1) reset in response to said reset signal such that a bus in said first bus segment is cleared from a hang condition (See col. 6, lines 31-35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Thus, House, as modified by Ehata, IBM_TDB and Looi, teaches said first bus is in said BUS FREE state (i.e., in fact that House teaches said computer system is using SCSI interface complying with SCSI standards, and said bus in said first bus segment is cleared from said hang condition implies that said first bus is in a BUS FREE state).

Referring to claims 13 and 25, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 13 and 25, respectively, except that does not teach said expander controller, which is said SCSI expander controller, enters into a reset isolation mode in response to said reset signal.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein an expander controller (e.g., bus expander bridge 50 of Fig. 1) enters into a reset isolation mode (i.e., reset state) in response to said reset signal (See col. 6, lines 26-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Referring to claims 16 and 27, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 16 and 27, respectively, except that does not teach a host computer on said first bus segment in said I/O subsystem, which is said SCSI I/O subsystem, asserts said reset signal on said first bus segment.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein a host computer (i.e., processor 20 of Fig. 1) in an I/O subsystem (i.e., computer system 10 of Fig. 1) on a first bus segment (i.e., Expansion bus 61 in Fig. 1) asserts a reset signal on said first bus segment (See col. 4, lines 12-16 and 42-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Referring to claims 18 and 29, House, as modified by Ehata and IBM_TDB, discloses all the limitations of the claims 18 and 29, respectively, except that does not expressly teach said bus segments are reset one segment at a time from said first bus segment.

Looi discloses an individually resettable bus expander bridge mechanism (See Abstract), wherein bus segments (i.e., Expansion bus 61 and Expansion bus 51 in Fig. 1) are reset one segment at a time from a first bus segment (i.e., Expansion bus 61 in Fig. 1; See col. 1, lines 6-10 and col. 6, lines 12-63).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said method steps (i.e., asserting said reset signal and resetting devices) in said mechanism, as disclosed by Looi, to said expander, as disclosed by House, as modified by Ehata and IBM_TDB, for the advantage of providing independently resetting said expander (i.e., bus expander bridge) in said I/O subsystem (i.e., computer system; See Looi, col. 2, lines 38-40).

Response to Arguments

6. Applicants' arguments filed on 26th of April 2004 (hereinafter the Response) have been fully considered but they are not persuasive.

In response to the Applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to the Applicants' argument with respect to Review of House As A Whole on page 17 in the Response, the Examiner believes that the Applicants misinterpret the claim rejection. The Applicants essentially argue that House does not teach two of the claimed steps [a) and b)] of the six steps claimed in the exemplary claim 1, and the claimed step c1) or c4) in the exemplary claim 1. However, said two of the claimed steps [a) and b)] are taught by Looi and Ehata (See the instant Office Action, page 3, line 4 through page 4, line 4), the claimed steps c1) through c4) are suggested by IBM_TDB (See the instant Office Action, page 4, lines 7-23). Even though the single reference House does not recognize an isolation between a pair of busses (e.g., main SCSI bus 26 and auxiliary SCSI bus 28 in Fig. 1), the combination of House and Ehata fully suggests the obviousness of "recognizing an isolation among a plurality of bus segments" (See the instant Office Action, page 3, lines 18-22). Furthermore, the Applicants essentially argue that House reference relied on in a rejection is inapplicable or cannot be combined because it does not appreciate Applicants' problem nor the claimed solution to that problem. In other words, it does not relate to solving the same problem that Applicants are addressing in its claimed invention (i.e., NOT the object of the claimed invention). The motivation to do what Applicants have done, however, does not have to be the same as the Applicants' to reach a conclusion of obviousness (See M.P.E.P. 2144). Moreover, the obviousness is not determined on the basis of purpose alone. *In re Graf,* 343 F.2d 774, 777, 145 USPQ 197, 199 (CCPA 1965). In summary, as long as there is

some suggestion/motivation within the prior art to make the modification or combination, it does not have to be the same as the Applicants'.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to Review of Looi As A Whole on page 18, and Review of Looi As A Whole: Claims 10 and 22 on page 19 in the Response, the Examiner believes that the Applicants misinterpret the claim rejection.

The Applicants essentially argue that Looi describes (1) a second bus segment (71, 72, with related devices), including the expander bridge 70, which is operably coupled to bus expander bridge 60 and is reset concurrently therewith at col. 5, lines 47-48, and (2) the direct connection between the first bus segment 60, 61, 62 and the second bus segment 70, 71, 72 acts to reset both the expansion bus 62 and the devices of the expander bridge 70 in response to the local bus reset signal 69 at col. 5, lines 60-65, and thus, (3) Looi is teaching away from the claimed isolation of the first and second bus segments.

The Examiner reminds the Applicants of the claimed subject matters "bus segment" being limited to have a set of devices and a bus that is coupled to the set of devices, and "expander" being limited to be arranged to couple a pair of busses (viz., to couple a pair of bus segments because each bus segment has a bus (i.e., single bus); See the preamble in the exemplary claim 1), and thus the expander should be arranged to couple the first bus segment and the second bus segment in light of the claimed invention. However, Looi does not support the claimed subject matter "expander", which should be arranged to couple the asserted first bus segment (i.e., bus expander bridge 60, expansion bus 61, and expansion bus 62) and the asserted second bus segment (i.e., compatibility bus expander bridge 70, compatibility bus 71, and bus reset 72). In other words, the Applicants' voluntary interpretation of Looi for the purpose of argument based on its second embodiment (Fig. 2) is not proper in light of the claimed invention. Instead, the Examiner's interpretation of Looi for the claim rejection based on its first embodiment (Fig. 1) is proper to teach/suggest that the claimed subject matter "expander" is arranged to couple the claimed

subject matter "first bus segment" and the claimed subject matter "second bus segment" because Bus Expander Bridge 60 (i.e., expander) is arranged to couple Expansion Bus 61 (i.e., the first bus segment) and Expansion Bus 62 (i.e., the second bus segment). Therefore, the Applicants' argument is not based on a sound interpretation of the Looi reference in light of the claimed invention, and Looi is not teaching away from the claimed invention.

Furthermore, even though the claimed isolation of the first and second bus segments is not expressly taught by Looi, Ehata suggests said claimed isolation (See the instant Office Action, page 3, lines 18-22). Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to Review of House As A Whole on page 20 in the Response, the Examiner respectfully reminds the Applicants that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, the claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over House in view of Ehata and IBM TDB (See paragraph 4 of the instant Office Action) by showing obviousness of the claimed invention.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "First, the goal of Ehata is understood by reference to paragraph 0005 and Figures 1 and 3. The Figures show one bus segment comprised of bus 3, many SCSI devices 2, and one host CPU 1. … Further does not describe or show any other bus segment … In contrast, not finding two clear claimed bus segments, the rejection breaks that one Ehata bus segment up into many asserted "bus segments", all of which are part of the one described 'one bus segment comprised of bus 3, many SCSI devices 2, and one host CPU 1'" on the Response page 20, line 21 through page 21, line 4, the Examiner respectfully reminds the Applicants that one cannot show

nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, the claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over House in view of Ehata and IBM TDB (See paragraph 4 of the instant Office Action) by showing obviousness of the claimed invention.

Furthermore, the Applicants essentially argue Ehata does not teach two clear claimed bus segments. However, House teaches said two clear claimed bus segments with expander (See the instant Office Action, page 6, line 11 through page 7, line 4). Ehata suggests the deficient element, i.e., the claimed subject matter "reset and segment isolation controller", and House in view of Ehata and IBM TDB with rationale for the proper combination suggests the obviousness of the claimed invention.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Initially, it is respectfully submitted that asserted Ehata first and second bus segments do not correspond to the claimed pair of first and second bus segments. ... Secondly, there is no assertion in the rejection (pages 9 and 11) that Ehata shows the claimed separate first and second I/O circuits that interface with the asserted respective first and second bus segments. ... Further, still viewing Ehata as a whole, ... In contrast, as claimed, the expansion controller is between the two claimed I/O interface circuits, one of which is connected to the first bus segment and one to the second bus segment." on the Response page 21, line 18 through page 22, line 19, the Examiner believes that the Applicants misinterpret the claim rejection.

The Applicants essentially argue that Ehata doesn't teach the above argued elements. However, House teaches the bus segment of main bus and the bus segment of auxiliary bus correspond to the claimed pair of first and second bus segments, and the expansion controller is between the two claimed I/O interface

circuits, one of which is connected to the first bus segment and one to the second bus segment (See the instant Office Action, page 6, line 11 through page 7, line 4).

Moreover, the claims 9 and 21 rejections under *35 USC §103(a)* in the prior and the instant Office Action established a *prima facie* case of obviousness meeting the three basic criteria of the MPEP 2143.03 (8th ed. 2001). And, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner has clearly pointed out rationale for appropriate combination of the references.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "After the abbreviated description of Ehata, the rejection attempted to justify the combination of Ehata and House ... It is respectfully submitted that to so characterize Ehata by equating a SCSI device with the claimed and defined bus segment improperly ignores the clear, as a whole teaching of Ehata of only one of the claimed 'bus segment'. ... The problem identified by Applicants is not appreciated by Ehata, ..." on the Response page 22, line 20 through page 23, line 4, the Examiner believes that the Applicants misinterpret the claim rejection.

In contrary to the Applicants' statement, the claim rejection clearly points out that House teaches said two clear claimed bus segments with expander (See the instant Office Action, page 6, line 11 through page 7, line 4), and Ehata suggests the deficient element, i.e., the claimed subject matter "reset and segment isolation controller".

Therefore, House in view of Ehata and IBM TDB obviously suggests all the limitations of the claimed invention in the claims 9 and 21, respectively (See paragraph 4 of the instant Office Action).

Again, the Examiner respectfully reminds the Applicants of the case law, "one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)."

Furthermore, in contrary to the Applicants' statement, Ehata teaches all of the devices of the first bus segment (i.e., all of the hung-up SCSI devices with the SCSI bus) are reset (i.e., clear bus hang) in response to the reset signal (i.e., RST signal) in light of the SCSI specification and Ehata's object of the invention.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "As noted, the Action asserted that the reset signal 6 is received on a first bus segment (a hung up SCSI device in Fig. 1, e.g., #1 device 2). … Viewing Ehata as a whole, the expander device that is to do the isolation from propagating must be part of that #2 not hung-up device 2 itself, because that #2 not hung-up SCSI device 2 is the asserted second bus segment. Moreover, any asserted isolation of the reset RST signal 6 must be isolation between the bus 3 (from which the RST signal 6 is received by #2 SCSI device 2) and the SCSI controller 4 of that #2 SCSI device 2 (which receives or does not receive an output from AND circuit 73 according to an input from OR circuit 72 and the RST signal 6) … Thus, the asserted expander device that is to do the isolating must be the 'reset-condition judging device 7'. However, in the context of claim 9, that #2 device 2 is part of one and the same claimed 'bus segment'." on the Response page 23, lines 5-18, the Examiner believes that the Applicants misinterpret the claim rejection.

The Applicants essentially argue that Ehata teaches the expander device that is to do the isolation from propagating must be part of that #2 not hung-up device 2 itself, because that #2 not hung-up SCSI device 2 is the asserted second bus segment, and thus the asserted second bus segment must be limited to only part of the not hung-up device.

However, it is noted that the features upon which applicant rely (i.e., isolation controller is not part of the second bus segment) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, the discussion regarding to the isolation controller is or is not part of the second bus segment is not a proper argument because it is not the features in the claimed invention. Furthermore, the argument is not based on the Examiner's interpretation of the prior art of record for the claim rejection, but the Applicants' voluntary interpretation of Ehata for the purpose of the argument.

In fact, Ehata suggests that the reset RST signal caused by the first bus segment (i.e., not hung-up device and SCSI bus) is isolated by the corresponding claimed subject matter "a reset and segment isolation controller" (i.e., reset-condition judging device) from propagating to the second bus segment (i.e., hung-up device and SCSI bus). In other words, Ehata describes (1) the first bus segment is not blocked by the reset-condition judging device for receiving the reset RST signal caused by the first bus segment, (2) the second bus segment is blocked by the reset-condition judging device for receiving the reset RST signal caused by the first bus segment at the same time (See paragraph [0007]), which implies that a reset and segment isolation controller isolates a reset signal received on the first bus segment from propagating to the second bus segment.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "... It is respectfully submitted that it is contrary to Ehata's teachings to isolate an operating SCSI device 2 (not hung-up) from all signals, because the whole purpose of not applying that one reset RST signal 6 to the operating SCSI device 2 is to allow that operating not hung-up device 2 to continue to operate independently of the hang-up of the other SCSI device 2 on that same bus segment (that includes the bus 3). Thus, consistent with the way Ehata is asserted, Ehata directly teaches that after isolating the reset signal from the not hung-up device 2,

one should allow all signals to be applied to that operating, not hung-up device so as to allow it to operate, e.g., in response to communication signals. As asserted, by allowing other signals from the bus 3 to reach the not hung-up device 2, Ehata teaches away from the claimed ..." on the Response page 23, line 19 through page 24, line 15, the Examiner believes that the Applicants misinterpret the applied reference and the claim rejection.

In contrary to the Applicants' assertion, Ehata does not disclose the whole purpose of not applying that one reset RST signal to the operating SCSI device is to allow that operating not hung-up device to continue to operate independently of the hang-up of the other SCSI device on that same bus segment. Instead, Ehata discloses the whole purpose of not applying that one reset RST signal to the operating SCSI device is to allow that having not hung-up offering the SCSI control circuit which avoids reset processing. Ehata is silent to mention if the whole purpose of not applying that one reset RST signal to the operating SCSI device is to allow that operating not hung-up device to continue to operate independently of the hang-up of the other SCSI device on that same bus segment. Therefore, in contrary to the Applicants' allegation, Ehata is not teach away from the limitation "said expander controller isolates all signals to prevent ..." in lines 15-17 of the exemplary claim 9, which is taught by IBM_TDB (See the instant Office Action, page 8, lines 1-9).

Thus, the Applicants' argument on this point is not persuasive.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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